PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

TOMITA et al.

Group Art Unit: Unassigned

Divisional of Parent
Application No.: 09/240,007

Examiner: Unassigned

Filed: Herewith

Attorney Dkt. No.: 100353-00029

For: SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Date: December 12, 2000

Sir:

Prior to initial examination of the application, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-42.

Please add new claims 43-48 as follows:

--43. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to the clock signal, said address-input circuit includes a delay circuit which operates in response to the clock signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the clock signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit; and

a bypass circuit provided in parallel to said delay circuit, wherein the address signals pass through the bypass circuit and bypass said delay circuit in a data-read mode.

44. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a strobe signal, the address-input circuit includes a delay circuit which operates in response to a clock signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the strobe signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit; and

a bypass circuit provided in parallel to said delay circuit, wherein the address signals pass through the bypass circuit and bypass said delay circuit in a data-read mode.

45. The memory circuit as claimed in claim 43, said delay circuit comprising a shift-register.

46. The memory circuit as claimed in claim 44, said delay circuit comprising a shift-register.

47. The memory circuit as claimed in claim 43, said delay circuit receiving latched address signals latched by the address-input circuit.

48. The memory circuit as claimed in claim 47, said delay circuit delaying the latched address signals for 1.5 clock cycles.--

REMARKS

Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300.

Respectfully submitted,

Rustan J. Hill
Registration No. 37,351

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W.,
Suite 600
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-481